What is claimed is:

1. A method for manufacturing a heterojunction bipolar transistor, comprising steps of:

providing a substrate;

forming a first at least one semiconductor layer on said substrate;

s; and

forming a second at least one semiconductor layer on said first at least one semiconductor layer; and

inserting a thermal treatment process within said second at least one semiconductor layer so as to improve a performance of said heterojuntion bipolar transistor.

2. The method according to claim 1, wherein said first at least one semiconductor layer comprises collector layers region, a base layer region.

3. The method according to claim 1, wherein said second at least one semiconductor layer comprises emitter layers region.

4. The method according to claim 1, wherein said first and second at least one layers are made of a material selected from a group consisting of a GaAs, an AlGaAs, an InGaP, an InGaAs, an AlInP, an InGaAs, an InAlAs, an InP, and a combination of III-V compound semiconductor materials thereof.

5. The method according to claim 1, wherein said thermal treatment process is performed at a temperature ranged from 300 °C to 800 °C.

6. A heterojunction bipolar device, comprising:

a substrate;

a first at least one semiconductor layer formed on said substrate;and

a second at least one semiconductor layer formed on said first at least one

semiconductor layer,

wherein a stack includes said substrate, said first at least one semiconductor layer, and said second at least one semiconductor layer, and a thermal treatment process is subjected to be inserted within said second at least one semiconductor layer so as to improve a performance of said heterojunction bipolar device.

7. The device according to claim 6, wherein said first at least one semiconductor layer comprises collector layers region, and a base layer region.

8. The device according to claim 6, wherein said second at least one semiconductor layer comprises emitter layers region.

9. The device according to claim 6, wherein said first and second at least one layers are made of a material selected from a group consisting of a GaAs, an AlGaAs, an InGaP, an InGaAs, an AlInP, an InGaAs, an InAlAs, an InP, and a combination of III-V compound semiconductor materials thereof.

10. The device according to claim 6, wherein said thermal treatment process is performed at a temperature ranged from 300 °C to 800 °C.